AMENDMENTS TO THE CLAIMS

1. – 12. (cancelled)

13. (currently amended) A method for protecting a gate terminal and lead at stage of scribing and spalling a liquid crystal panel, said method comprising:

providing a first substrate;

forming ~~the~~ a gate electrode and ~~the~~ a gate electrode line on said first substrate, wherein said gate electrode line comprises said gate terminal and said lead;

depositing a blanket gate insulating layer on said gate electrode, said gate electrode line, and said first substrate;

forming an island semiconductor layer on said gate electrode, ~~and~~ a source electrode and a drain electrode on said island semiconductor layer, and ~~simultaneously forming~~ a resist region on said gate insulating layer ~~and covering,~~ wherein said resist region covers said gate terminal and said lead ~~of a gate electrode line, said resist region~~ and is located at a scribing line on margin of a second substrate with color filter thereon; and

depositing a blanket passivation layer on said source electrode, said drain electrode, and said resist region.

14. (original) The method according to claim 13, wherein said resist region is formed of metal.

15. (original) The method according to claim 14, wherein said resist region is floating.

16. (currently amended) The method according to claim ~~15~~ 13, wherein said step of formation said ~~floating metal~~ resist region is at a step of formation of said source electrode and said drain electrode.

17. (currently amended) The method according to claim 16, wherein formation of said ~~floating metal~~ resist region comprises:

forming ~~an~~ said island semiconductor layer on said gate insulating layer and over said gate electrode;

depositing a blanket metal layer on said island semiconductor layer and said gate insulating layer;

performing a lithographic process to said conductive layer by using a reticle with a source pattern and a drain pattern on said gate electrode and a resist region pattern on said gate terminal and said lead; and

etching said conductive layer to form said source electrode, said drain electrode and said ~~floating metal~~ resist region.

18. (currently amended) The method according to claim ~~15~~ 13, wherein ~~activity of said floating metal resist region is less than~~ said gate electrode line is more active than said resist region.

19. (currently amended) The method according to claim ~~15~~ 13, wherein distance between said scribing line and margin of said ~~floating metal~~ resist region is ~~about~~ more than 50 μm.

20. (currently amended) The method according to claim 19, wherein width of said ~~floating metal~~ resist region is larger than those of said gate terminal and said gate electrode line.